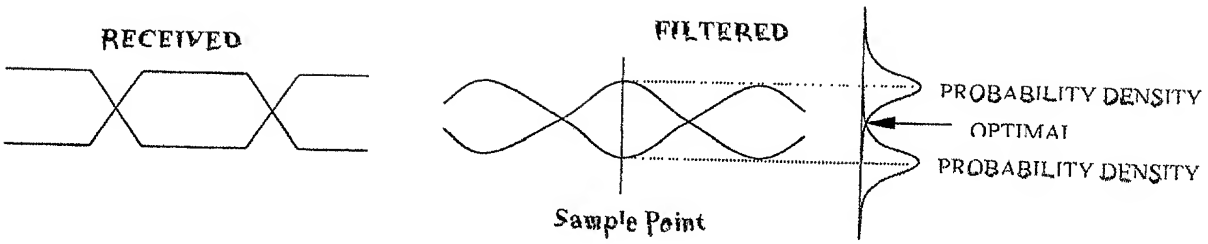


Fig. 1 (prior art)

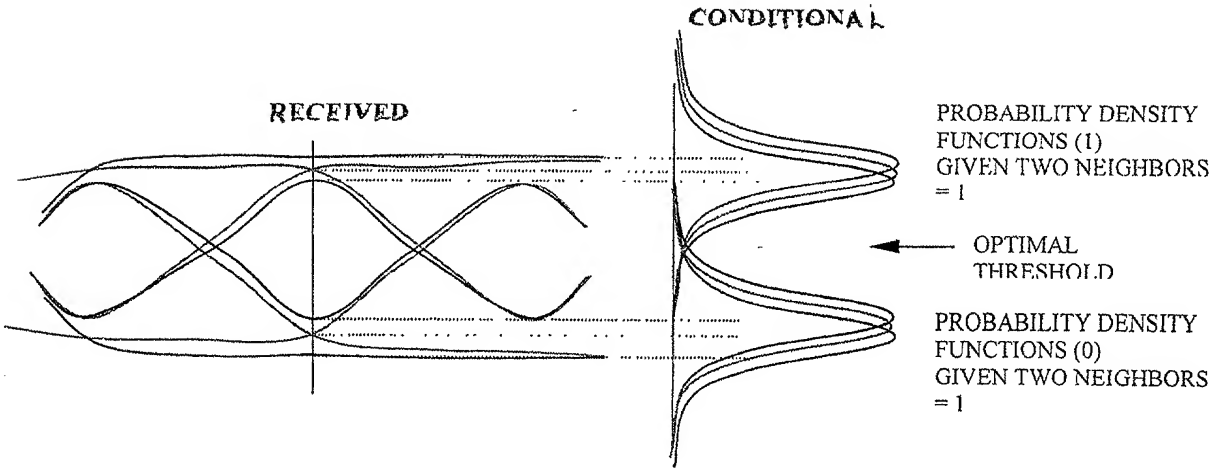


Fig. 2 (prior art)

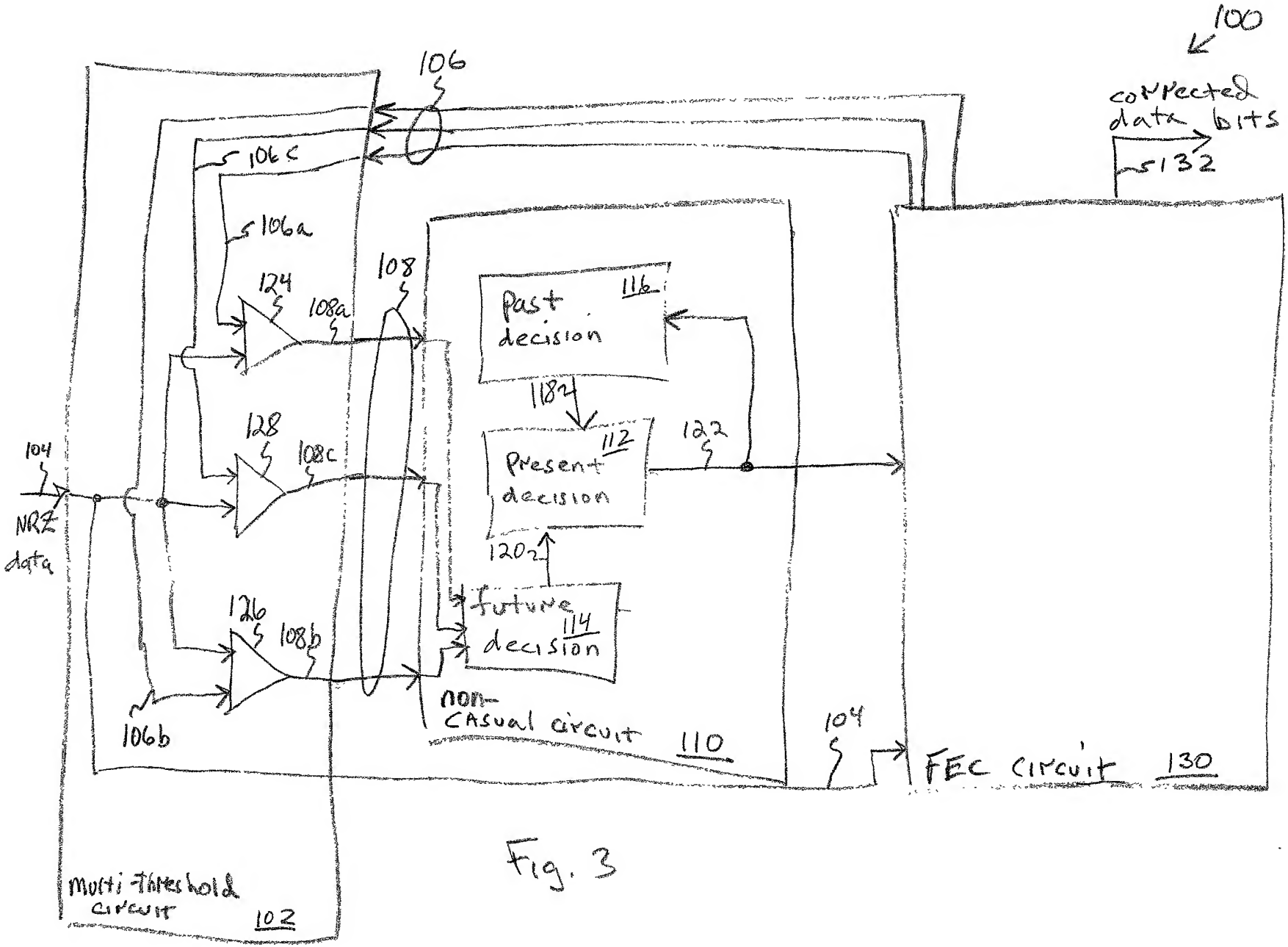

100
106
corrected data bits
132
106c
106a
124
108a
108
past decision
116
118a
112
present decision
122
128
108c
104
NRZ data
120a
future decision
114
126
108b
106b
non-CASual circuit
110
104
FEC circuit
130
Multi-threshold circuit
102

Fig. 3

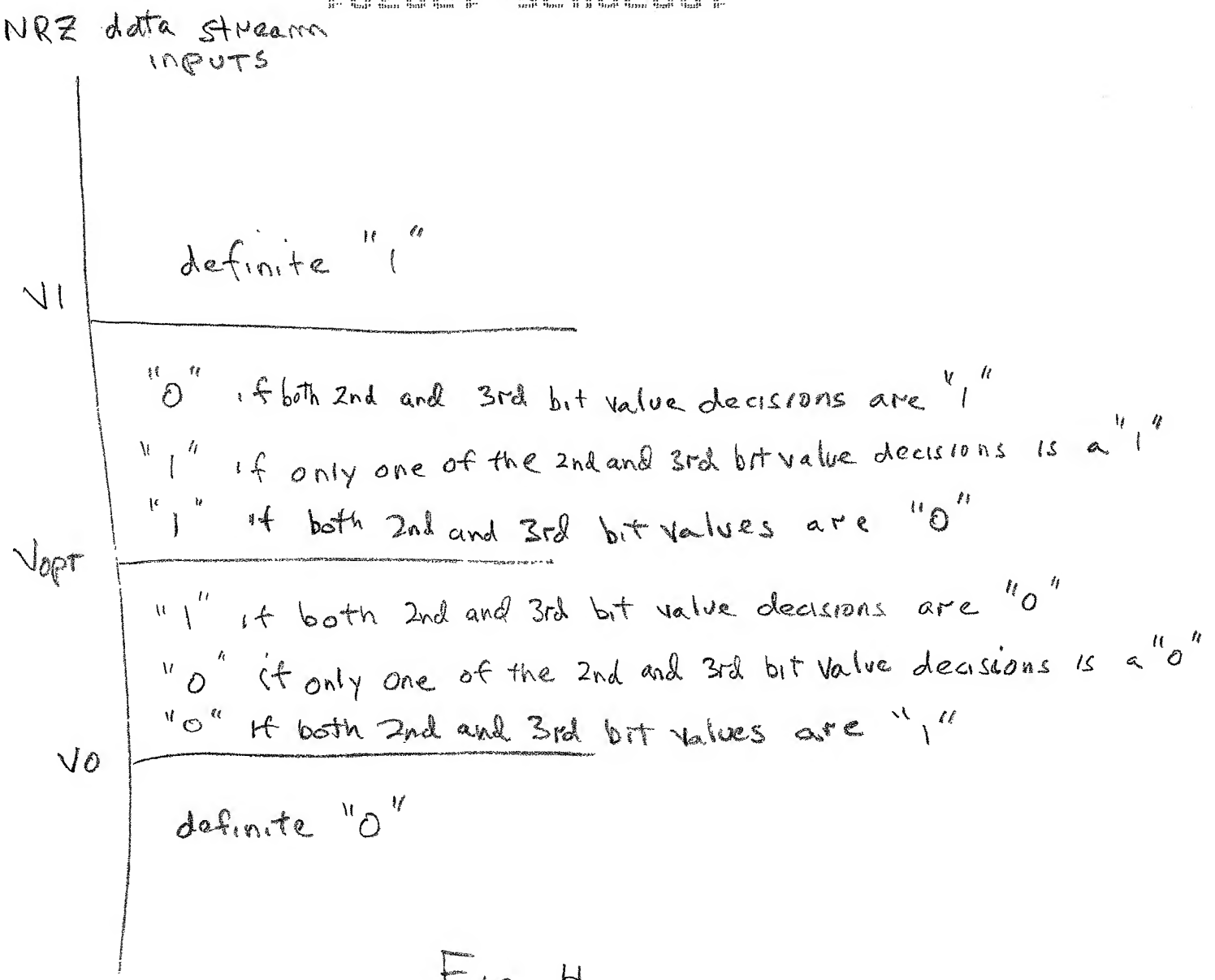

NRZ data stream
INPUTS
definite "1"
V1
"0" if both 2nd and 3rd bit value decisions are "1"
"1" if only one of the 2nd and 3rd bit value decisions is a "1"
"1" if both 2nd and 3rd bit values are "0"
Vopt
"1" if both 2nd and 3rd bit value decisions are "0"
"0" if only one of the 2nd and 3rd bit value decisions is a "0"
"0" if both 2nd and 3rd bit values are "1"
V0
definite "0"

Fig. 4

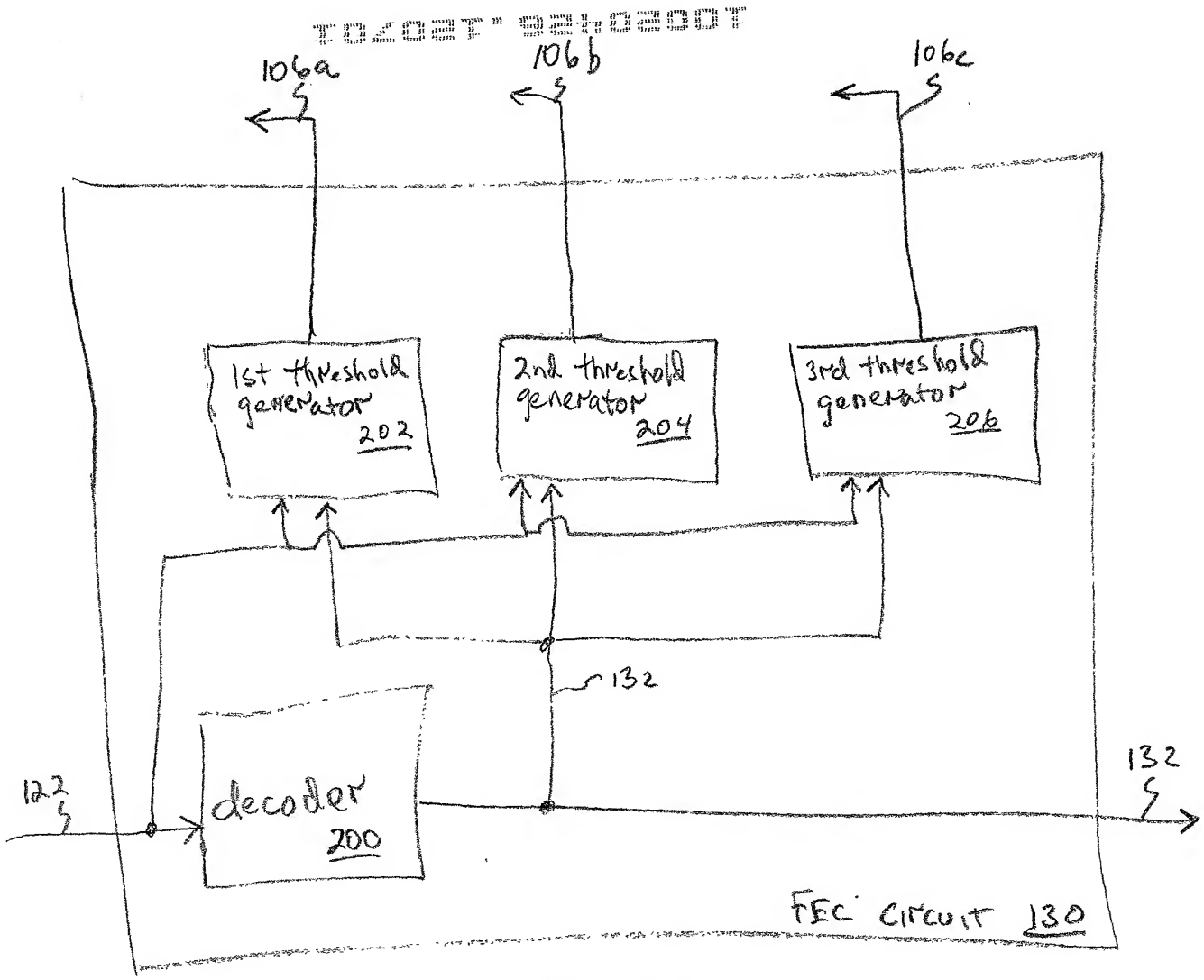

106a
106b
106c
1st threshold generator 202
2nd threshold generator 204
3rd threshold generator 206
132
122
decoder 200
132
FEC circuit 130

Fig. 5

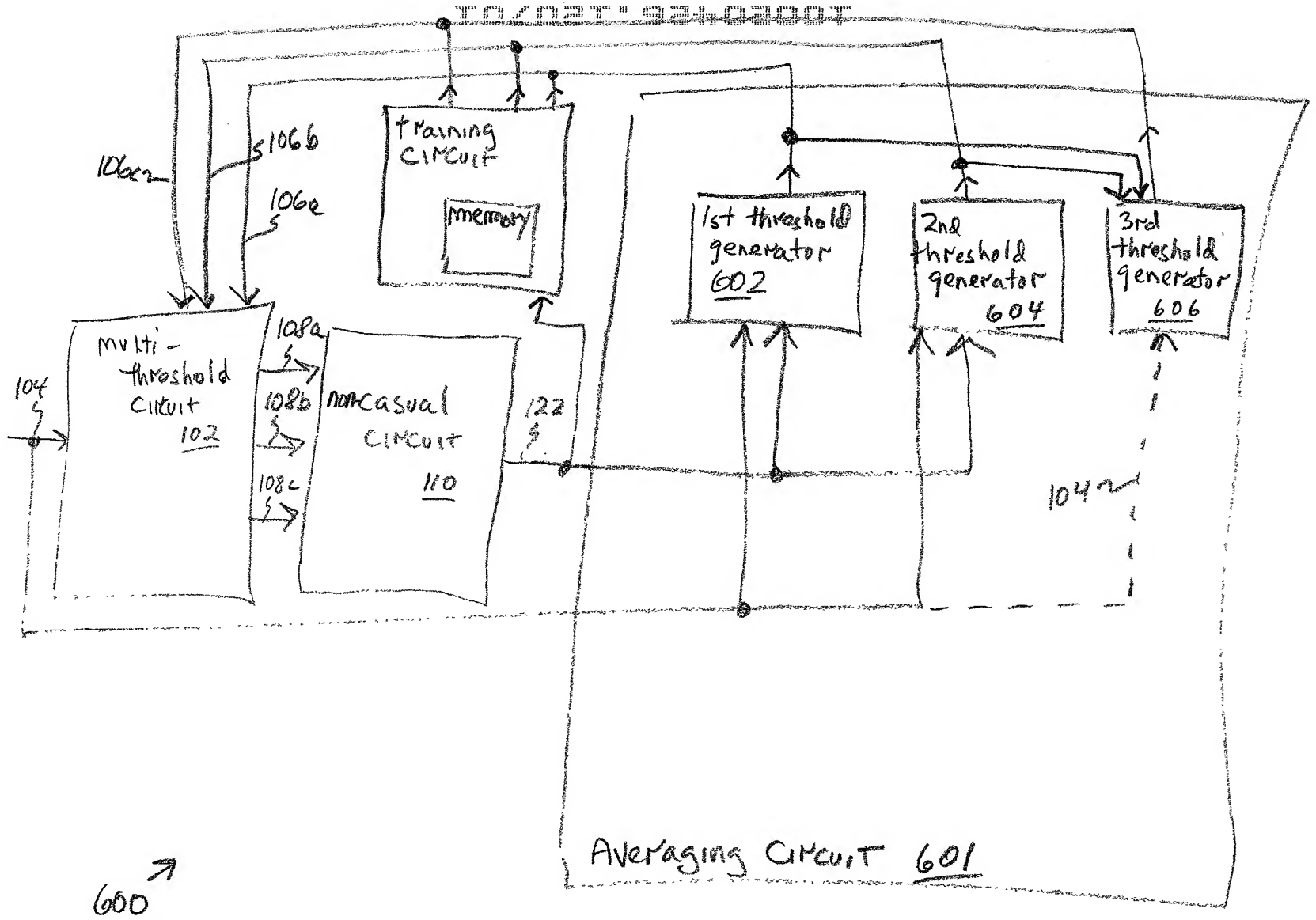
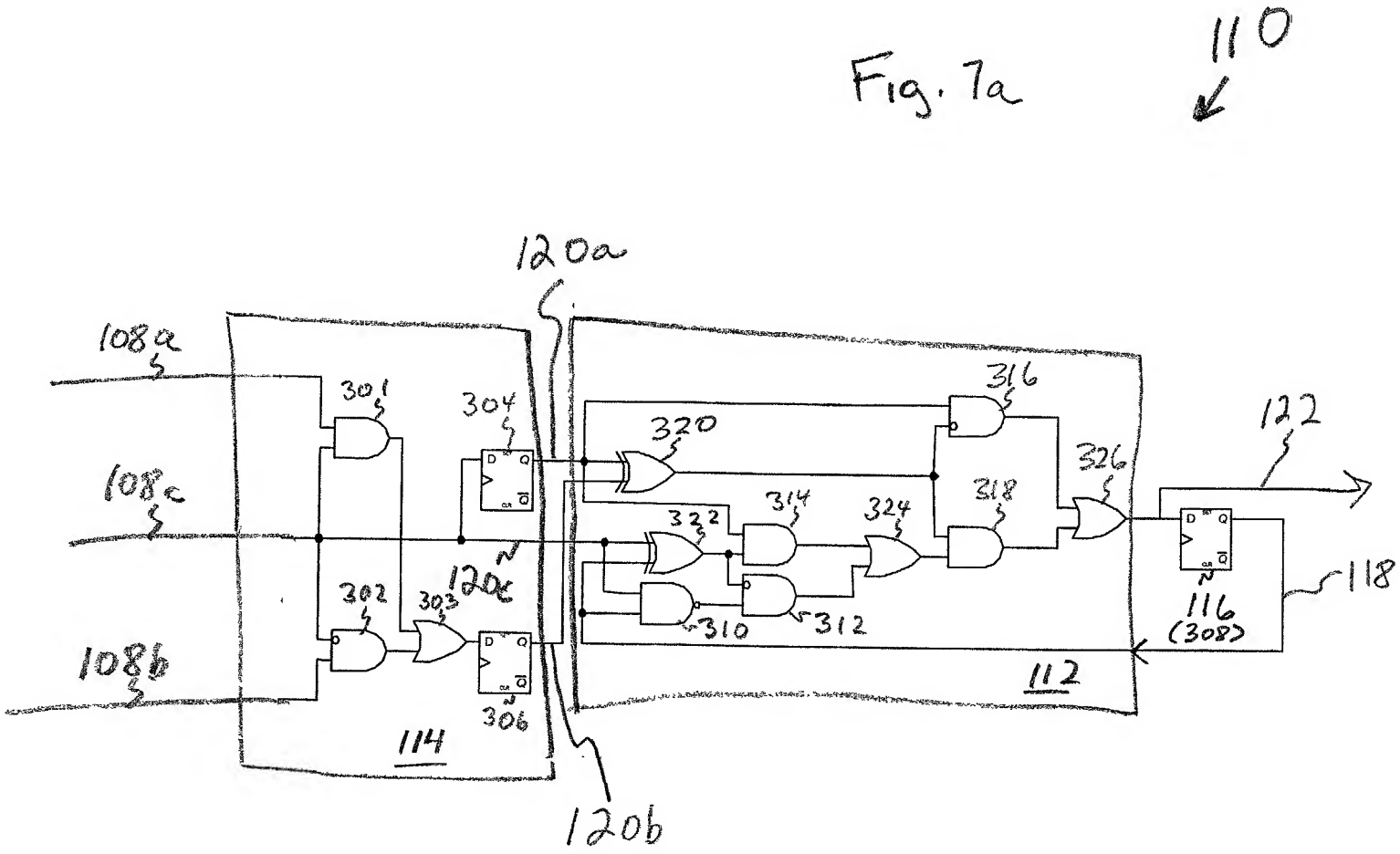

training circuit
memory
1st threshold generator 602
2nd threshold generator 604
3rd threshold generator 606
multi-threshold circuit 102
noncasual circuit 110
106a
106b
106c
108a
108b
108c
104
122
Averaging circuit 601
600

Fig. 6

Fig. 7a


110
120a
108a
108c
108b
301
304
320
316
122
326
318
314
324
322
120c
302
303
310
312
116
(308)
118
306
114
112
120b

FIRST BIT Estimate		2nd bit Value	3rd bit value	1st bit Value
line 120a	120b			
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Fig. 7b

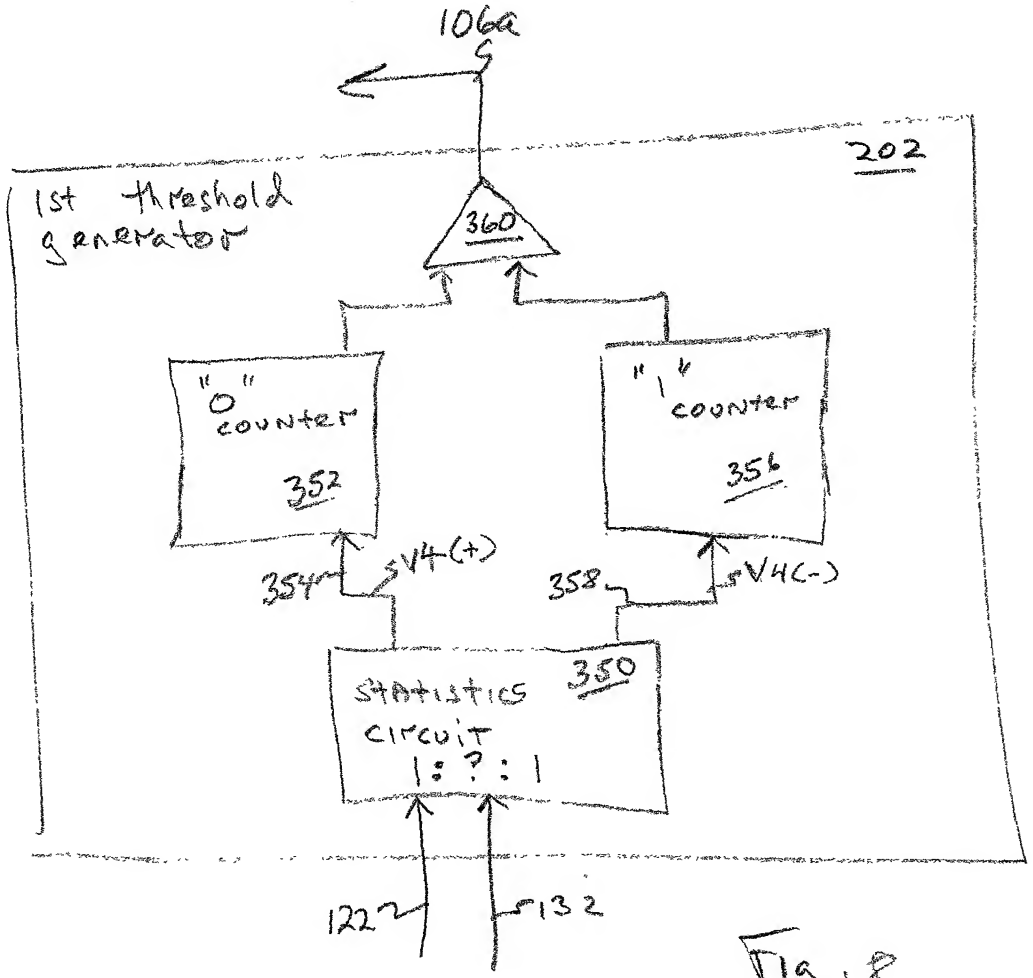


Fig. 8

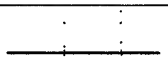
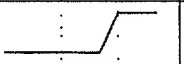
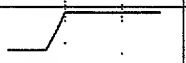
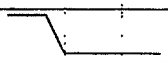
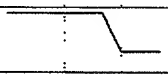
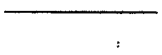
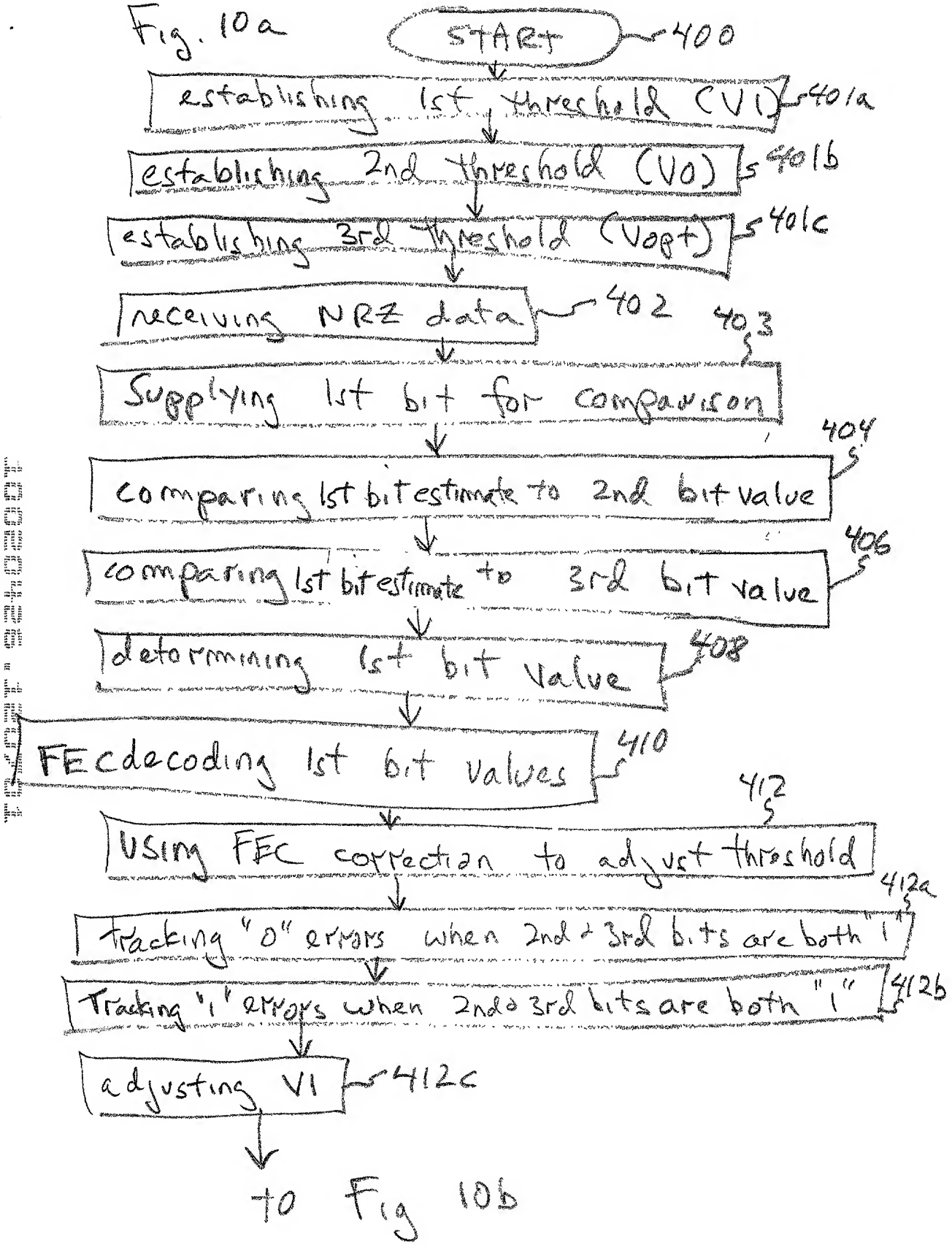
Only One Correction per 3 bit sequence Error in the center bit					
Corrected Sequence	**Graphic**	**Affected Counter**		**Action on Feedback**	
OK-ER-OK		0 cntr	1 cntr	-	+
0 0 0		Cond 1 0 inc		V1 toggle	
0 0 1		Cond 2 0 inc		V2 toggle	
0 1 0			Cond 1 1 inc		V1 Toggle
0 1 1			Cond 2 1 inc		V2 Toggle
1 0 0		Cond 3 0 inc		V3 Toggle	
1 0 1		Cond 4 0 inc		V4 Toggle	
1 1 0			Cond 3 1 inc		V3 Toggle
1 1 1			Cond 4 1 inc		V4 Toggle

Fig. 9

Fig. 10a


START
400
establishing 1st threshold (V1)
401a
establishing 2nd threshold (V0)
401b
establishing 3rd threshold (Vopt)
401c
receiving NRZ data
402
403
Supplying 1st bit for comparison
404
comparing 1st bit estimate to 2nd bit value
406
comparing 1st bit estimate to 3rd bit value
408
determining 1st bit value
410
FEC decoding 1st bit values
412
using FEC correction to adjust threshold
412a
Tracking "0" errors when 2nd & 3rd bits are both "1"
412b
Tracking "1" errors when 2nd & 3rd bits are both "1"
412c
adjusting V1
to Fig 10b

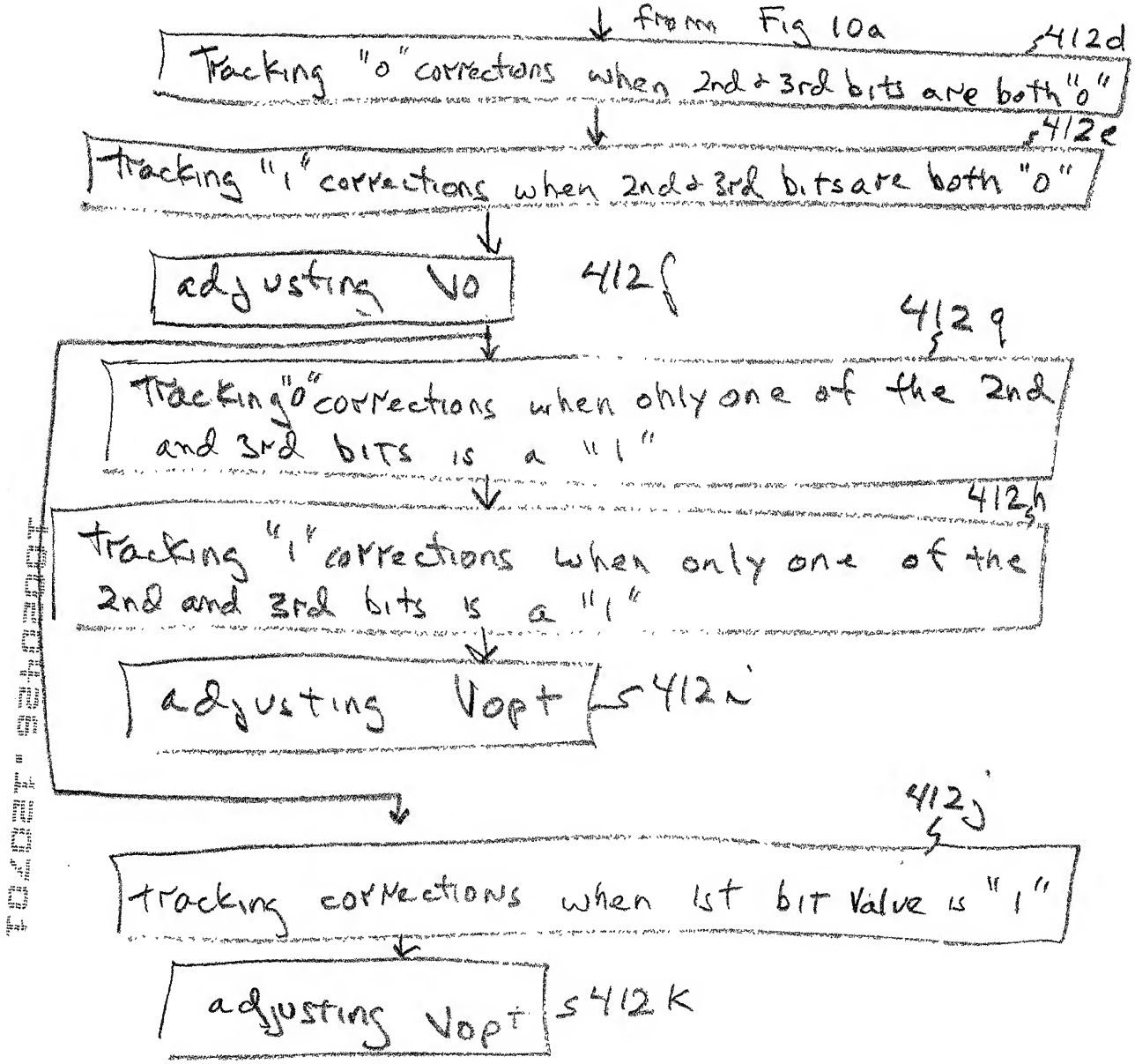
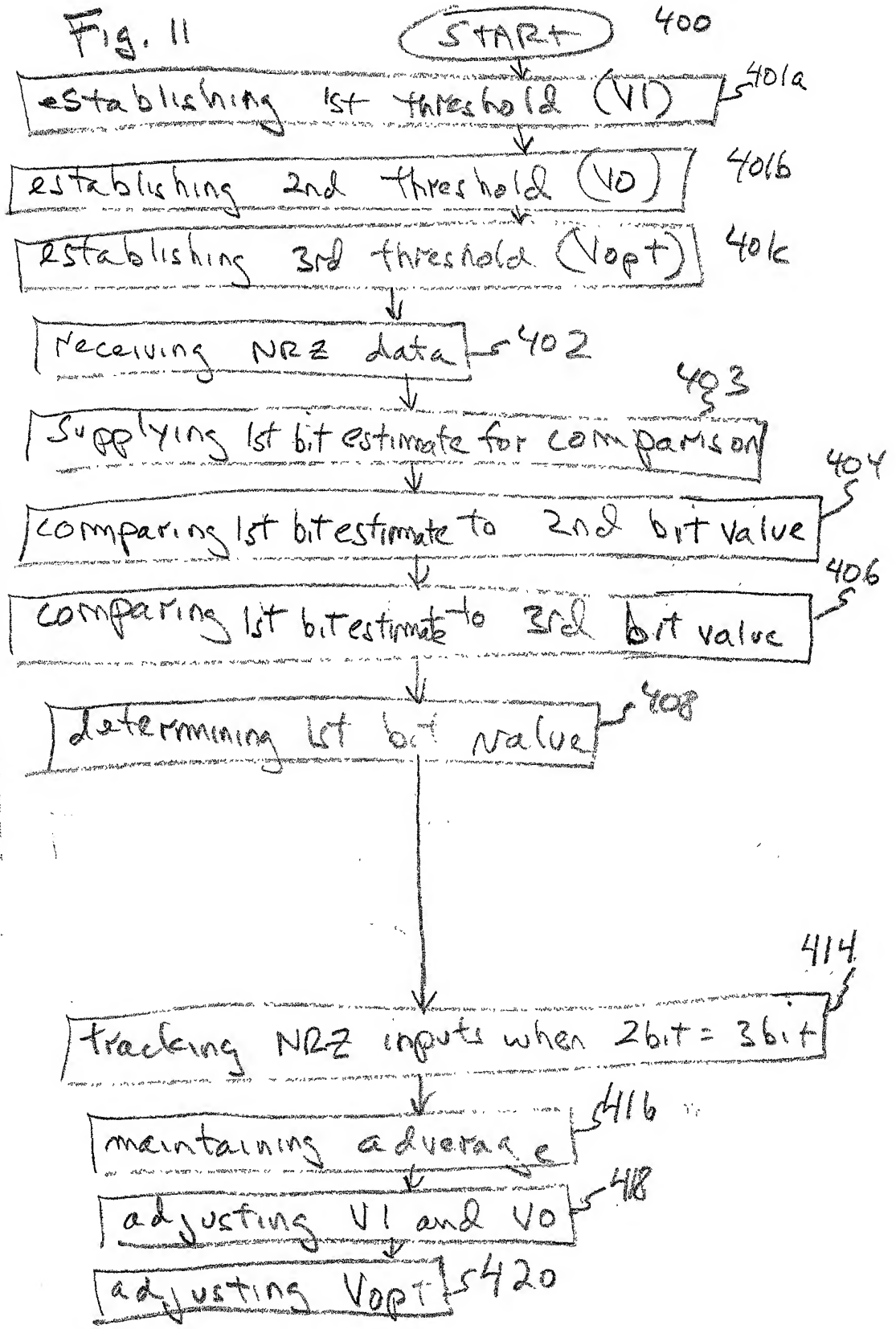

from Fig 10a
412d
Tracking "0" corrections when 2nd & 3rd bits are both "0"
412e
Tracking "1" corrections when 2nd & 3rd bits are both "0"
adjusting V0
412f
412g
Tracking "0" corrections when only one of the 2nd and 3rd bits is a "1"
412h
Tracking "1" corrections when only one of the 2nd and 3rd bits is a "1"
adjusting Vopt
412i
412j
tracking corrections when 1st bit value is "1"
adjusting Vopt
412k

Fig. 10b

Fig. 11


START
400
establishing 1st threshold (V1)
401a
establishing 2nd threshold (V0)
401b
establishing 3rd threshold (Vopt)
401c
receiving NRZ data
402
supplying 1st bit estimate for comparison
403
comparing 1st bit estimate to 2nd bit value
404
comparing 1st bit estimate to 3rd bit value
406
determining 1st bit value
408
tracking NRZ inputs when 2bit = 3bit
414
maintaining average
416
adjusting V1 and V0
418
adjusting Vopt
420

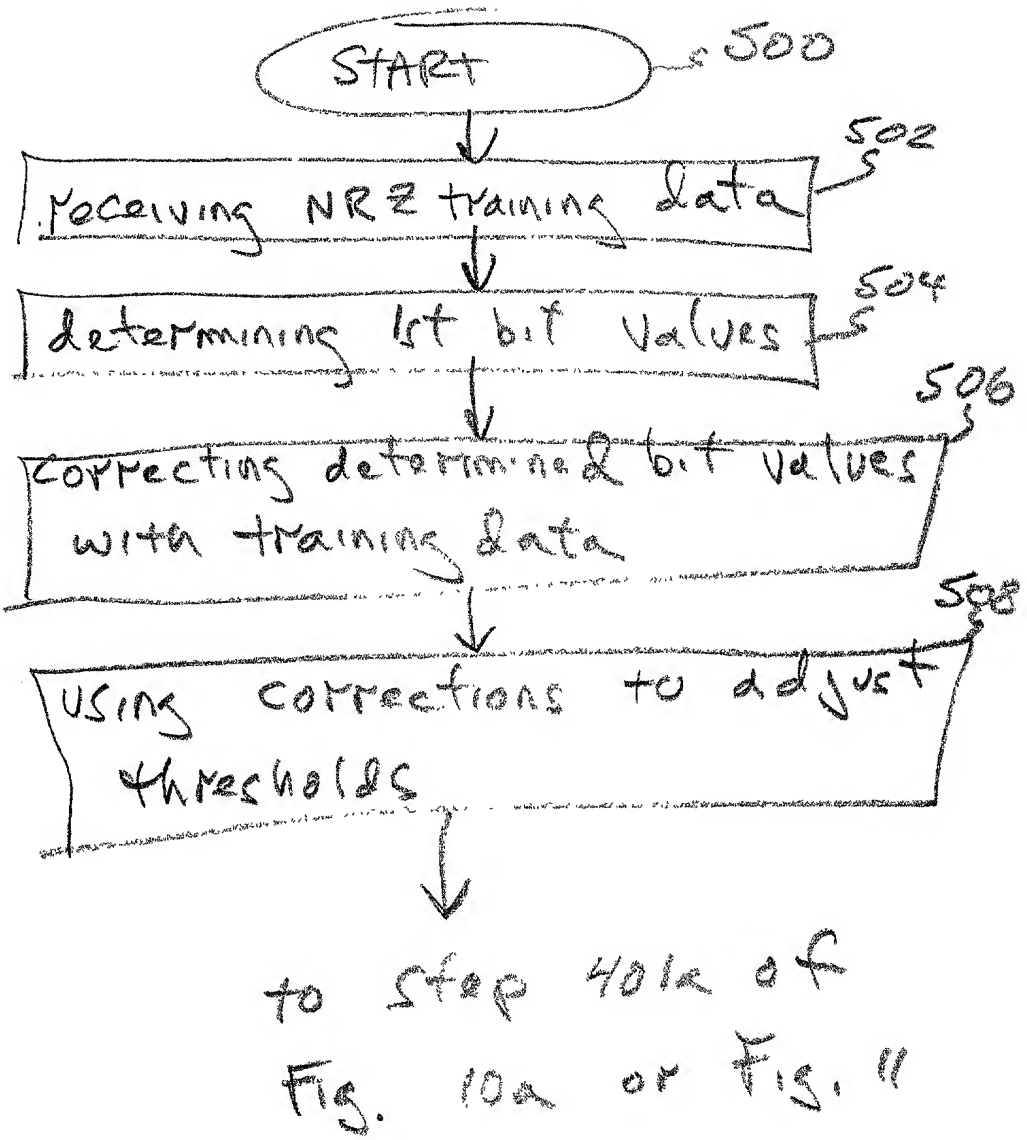

START
500
receiving NRZ training data
502
determining 1st bit values
504
correcting determined bit values with training data
506
using corrections to adjust thresholds
508
to step 404a of Fig. 10a or Fig. 11

Fig. 12